Study of multi-ON states in nonvolatile memory based on metal-insulator-metal structure

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Various mechanisms have been proposed to interpret switching effect in thermally evaporated organic memory devices. In this work, we demonstrate a nonvolatile memory device having tristates, one OFF state and two different ON states (lower-ON state, higher-ON state) in the metal-insulator-metal (MIM) structure. Detailed study has revealed that different switching mechanisms are responsible for these two stages of switching: filament formation is the dominant mechanism for switching from the OFF state to the lower ON state while Poole–Frenkel effect governs the switching from the lower-ON state to the higher-ON state. © 2009 American Institute of Physics. [doi:10.1063/1.3263155]

Since the publication of Hickmott’s investigations on current-voltage characteristics of metal-oxide-metal trilayer structure, there have been considerable researches in the thin-film metal-insulator-metal (MIM) devices. In these studies, a range of different insulating materials made of inorganic as well as organic elements was sandwiched between two metal electrodes, and switching between different conductance states could be achieved by applying suitable voltages. The underlying physical mechanism of MIM switching has been investigated by a number of researchers, and different explanations have been proposed to interpret the switching mechanism. Poole–Frenkel-like charge transport, involving donors, and neutral traps, which originate from structural defects in thin film, is common in electronic devices fabricated by thermal evaporation. In 1972, Gundlach and Kadlec proposed that the switching was actually independent of materials. In after years, extensive research has shown that the device performance actually depends on the sample preparation methods and electrode deposition conditions. Based on experimental results, it has been speculated that filamentary paths, which exist in the insulating matrix, dominate the electrical conductivity.

In this manuscript, we report a nonvolatile memory device containing one OFF state and two different ON states with thin-film MIM structure. This device could switch from the OFF state to the lower ON state (LON) or from the LON state to the higher ON state (HON) by proper bias exceeding a critical voltage \( V_C \), which is indicative of the domination of different conduction mechanisms in these two regions. There is no direct transition from the OFF state to the HON state in a single sweep. Detailed experimental results suggest that more than one physical process is involved in switching and two ON states are dominated by different conduction mechanisms. Our work is not limited to proposing the critical voltage \( V_C \), but it also helps us to further understand the physical principle of switching phenomenon in electronic devices fabricated by thermal evaporation.

A 20 nm thick Au layer was deposited onto the glass substrate at a rate of 0.5 Å/s, followed by a 100 nm thick silicon monoxide layer evaporated at a rate of 1 Å/s. The last layer was 20 nm thick Au layer serving as the top electrode. All the insulator layers and electrodes were deposited at pressure lower than \( 2 \times 10^{-6} \) torr. After the evaporation, the vacuum was broken and the device was transferred into cryogenic probe station (Janis Corporation) for electrical measurements. All electrical measurements were done under a pressure lower than \( 10^{-3} \) torr in the probe station at room temperature.

The current-voltage curves in Fig. 1 clearly show three states including the OFF state, the LON state, and the HON state. The applied bias was performed in the following sequence. First, during the voltage sweep from 0 to 4 V, the device was initially in the OFF state characterized by a low current less than \( 10^{-7} \) A. Once a certain threshold voltage \( V_{th1} \approx 3.8 \) V was exceeded as shown in Fig. 1, the electrical current abruptly jumped to \( 1 \times 10^{-3} \) A, a four orders of magnitude rise. The device was now switched from the OFF state to the LON state. The second voltage scan from 0 to 6 V showed linear I-V characteristic for the device in the LON state. To switch the device to the HON state, a write voltage higher than \( V_{th2} \approx 2.6 \) V was necessary. The third scan from

![FIG. 1. (Color online) I-V performance shows one OFF state and two ON states. The inset is a schematic drawing of a typical memory device structure.](image-url)
0 to 10 V showed the HON I-V behavior, followed by a negative differential resistance (NDR) region where current decreased with increasing voltage. At the end of 10V ramp, the device returned back to the OFF state.

The further exploration of I-V characteristic of the device is shown in Fig. 2. A bias of approximately 4V switched the device to the LON state. Any scan less than 5.2 V gave a linear I-V curve at this stage in the LON region marked as (a). But, at bias greater than critical bias ($V_{C} \approx 5.2$ V), the I-V characteristic changed to parabolic marked as (b) in Fig. 2. A voltage greater than $V_{th1}$ at this stage switches the device to the HON state. Normally $V_{th2} < V_{th1} < V_{C}$. The device would not be turned to the HON state unless a bias larger than the $V_{C}$ was applied when the device was in the LON state. Temperature-dependence measurements for the device in the LON State show negligible change in the current under 1 V (as shown in inset of Fig. 2), implying filament formation as the dominating conductive mechanism. Calculations have found that in the region of high electric fields, the I-V performance in the HON state complied with Poole-Frenkel [\(\ln(I) \propto \sqrt{V}\)] conduction mechanism. A detailed explanation will be discussed in later sections.

As shown in Fig. 3, multistable states could be obtained by applying a proper erasing voltage in the NDR region, all of which have a common feature of a “current bump.” This phenomenon has also been observed by other researchers. It is worth mentioning here that even though some multilevel states had the same current value as the LON state under small reading voltage (1 V), the voltage ramp clearly showed different I-V characteristics. This implied that the multilevel states and the LON state phenomenon have different mechanisms.

A HP-4284A precision LCR meter was used to analyze the impedance of each of these states. A model of a capacitor with capacitance $C$ and a resistor with resistance $R$ connected in parallel was introduced to interpret the measurements. Equation (1) describes the influence of $C$ and $R$ on the absolute value of impedance $|Z|$ as well as the phase angle $\theta$.

$$|Z| = \frac{1}{\sqrt{\frac{1}{R^2} + \omega^2 C^2}} \quad \theta = -\text{atan}(\omega CR).$$

We define the low frequency region from 10 to $10^5$ Hz and a high frequency region from $10^3$ to $10^6$ Hz. In Fig. 4(a), when the device is in the OFF state, $R$ has such a large value that the impedance is mainly dominated by the capacitance part. The device in both the LON state and the HON state shows frequency independence when it is lower than $10^3$ Hz, implying the resistance part contributes more to the overall characteristics of impedance spectra in comparison to the capacitance part. Figure 4(b) shows the capacitance values normalized to the capacitance of the OFF state at high frequency. Curve I, depicting the behavior at high frequency shows negligible change for each of the states. However, curve II, depicting the behavior at low frequency shows an order of magnitude increase of capacitance on switching from the LON state to the HON state. This also suggests that a different mechanism was involved in the switching.

All of the phenomena presented above are considered to be due to the fabrication process of our device as well as the intrinsic property of vacuum-deposited SiO films. The gold diffusion characteristic, which has been shown by many researchers, is considered to be the reason for the existence of dispersed metal island in the insulator matrix. Meanwhile, the SiO compounds would inevitably dissociate during the vacuum deposition and yield SiO$_2$ and free Si, which result in the high trap density in the amorphous SiO film. The whole device could be thought as a SiO matrix containing neutral traps and donors in between Au electrodes.

To address these reliable experiment evidences, a model of combining filamentary formation as well as “anomalous” Poole–Frenkel effect was presented. When the voltage is initially increased, the local electrode metal is transported into the insulator. A highly conductive filamentary path could be formed as the voltage is in excess of $V_{th1}$. The current would flow across the conductive filamentary path that explains the linear I-V relationship of the device in the LON state. The unchanged capacitance from the OFF state to the LON state further supports the existence of filamentary path. The filamentary path would not be burned unless an even larger bias ($>V_{C}$) is applied. As the voltage reaches
and COFF−High f represents the capacitance of the device in the OFF state.

Different states. C represents the capacitance of the device in different states, tested under high frequency.

Under the high erase voltage, the electrons are swept out of the traps and the Au donors are reneutralized, which leads to an overall decrease in current. The device is turned back to the OFF state.

In summary, we have experimentally demonstrated a nonvolatile multilevel memory with inorganic thin-film MIM structure. Experimental investigation of the L_{ON} state implies that a critical voltage V_C is required to be surpassed in order to obtain the H_{ON} state. ac behaviors of the device under different conductive states are consistent with the proposed mechanism, which suggest more than one physical process are involved. To further prove the physical principles in our device, more experiments are being carried out. This work provides a possibility for further understanding the physical principle and mechanism in electronic devices fabricated by thermal evaporation method.

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\[ \text{Curves I and II represent the capacitance of the device in different states, and } \text{C}_{\text{OFF-High f}} \text{ represents the capacitance of the device in the OFF state tested under high frequency.} \]

\[ \text{FIG. 4. (Color online) Impedance measurements of the device in different conductive states. (a) The top and the bottom figures show the phase angle } \theta \text{ and the absolute value of the impedance } |Z| \text{ with respect to the frequency, respectively. The inset draws the model of a capacitor and a resistor connected in parallel. (b) Capacitance ratio of } C \text{ to } \text{C}_{\text{OFF-High f}} \text{ with respect to different states. } C \text{ represents the capacitance of the device in different states, and } \text{C}_{\text{OFF-High f}} \text{ represents the capacitance of the device in the OFF state tested under high frequency.} \]