Unique architecture and concept for high-performance organic transistors

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We report an organic transistor with a vertically stack structure, which consists of a layer-by-layer active cell (drain/organics/source) on top of a capacitor cell (source/dielectrics/gate); the middle source electrode is shared by the capacitor cell and active cell. Three unique characteristics of this transistor, (a) its very thin and rough middle source electrode; (b) its capacitor cell with high charge-storage capability, allow the active cell to be influenced when the gate is biased; and (c) the large cross-section area and small distance between the source and the drain allow current flowing between the source and drain electrodes. Devices have been fabricated by thermal evaporation with the source-drain current well modulated by the gate potential. We have achieved organic transistors with low working voltage (less than 5 V) and high current output (up to 10 mA or 4 A/cm^2) and an ON/OFF ratio of 4×10^6. A model is proposed for the device operation mechanism. The demonstrated device with its enhanced operating characteristics may open directions for organic transistors and their applications. © *2004 American Institute of Physics*. [DOI: 10.1063/1.1821629]

Organic field effect transistors (OFETs) and thin film transistors have attracted considerable attention since their discovery[1,2] due to their flexibility, low cost, and amenability to fabrication over large surface areas. They have been extensively investigated.[3,4] However, the performance of OFETs is still poor compared to their inorganic counterparts, showing low current output (on the order of μA) and high working voltages (up to 100 V) in general.[4,5] Some approaches to enhance the OFETs' performance, such as decreasing the channel length and increasing the dielectric constant of the gate dielectrics, have been reported.[6–11] However, the performance is still quite limited. In this letter, we demonstrate an organic field effect transistor that utilizes a vertically stacked structure with promising performance.

Figure 1(a) shows a schematic diagram of the device structure. It consists of an active cell on top of a capacitor cell. The middle electrode is defined as the common-source electrode, which is very thin and rough (the roughness is comparable to its thickness). The top electrode and the bottom electrode are defined as the drain and gate electrode, respectively. The operating principal of our device, which will be discussed later, requires two important conditions to be satisfied simultaneously, (a) a thin and rough source electrode, and (b) a high capacitance for the bottom capacitor cell. Figure 1(b) shows an atomic force microscope (AFM) image of the surface of the source electrode for our device, indicating its granular structure and high roughness. Figure 1(c) shows the high capacitance of the bottom capacitor cell, and the inset of Fig. 1(c) shows the humidity dependence of the capacitance of the capacitor cell for our devices, suggesting solid-state electrochemical supercapacitor formation. This device structure provides, intrinsically, a very short "channel length" between the source and drain electrode and an extremely large cross-sectional area, allowing the possibility for low working voltages and high current outputs. We define this device as a gate-source-drain vertical organic field effect transistor (VOFET).

Vacuum thermal evaporation methods were used for device fabrication. Materials were purchased from Aldrich and they were used as received. Copper (Cu) was first deposited on a precleaned glass substrate as the bottom gate electrode. The lithium fluoride (LiF) layer, 240 nm thick, followed as the gate dielectric layer. Cu(20 nm)/Al(10 nm) was deposited next as the source electrode. C_{60} was deposited on top of the source electrode as the active organic layer. Finally, the top electrode was deposited to complete fabrication of the device. The device area (0.25 mm^2) was defined by the crossover between the drain and source electrodes.

Drain-source current–voltage (I_{sd}–V_d) characteristics at various gate potentials for a VOFET with C_{60} as the organic layer and Cu/Al as the source electrode are shown in Fig. 2(a). For this device the current output is near 10 mA (or 4 A/cm^2) at working voltage less than 5 V. It should be mentioned that the leakage current from gate to source is in

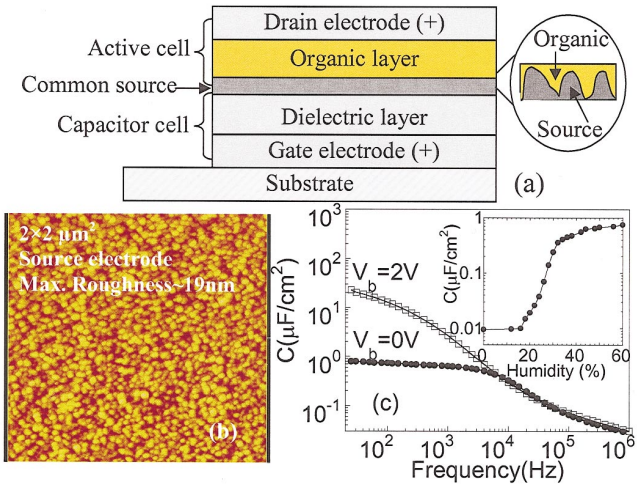

FIG. 1. (Color) (a) The schematic diagram of the proposed device structure. (b) atomic force microscope image of the surface of the source electrode. (c) The frequency dependence of the capacitance for the capacitor cell with ambient relative humidity of 44%. The inset is the ambient relative humidity dependence of the capacitance for the capacitor cell at 25 Hz without dc bias.

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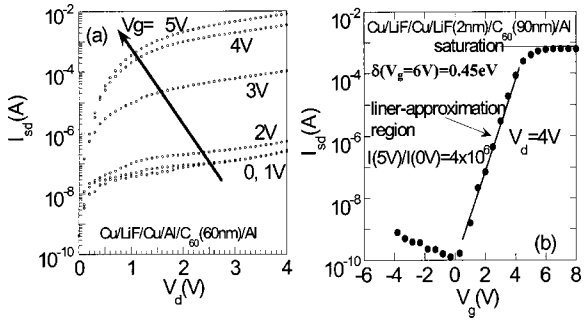

FIG. 2. (a) The $I_{sd}-V_d$ characteristics of a VOFET at various gate biases. (b) The $I_{sd}-V_g$ characteristics at $V_d=4$ V for a VOFET with LiF buffer layer at the source/C_{60} interface.

the μA range. The ON/OFF ratio (current ratio at certain drain voltage with and without gate bias) at 5 V gate bias and 4 V drain bias is near 4×10^6 [Fig. 2(b)].

The transistor operates in the following fashion. An *n*-type organic semiconductor is used for the active cell. The source electrode is used as a common cathode for both the capacitor cell and the active cell. Consequently, the current injection for the active cell is controlled by electron injection from the source electrode. We selected materials with mismatched energy levels between the organic semiconductor and the source electrode at zero gate-bias condition in order to achieve low leakage current. This approach is similar to that of a Schottky barrier transistor.[13] We focus on the interface between the source electrode and the organic semiconductor layer to demonstrate the device working principle (Fig. 3). Before applying a gate bias [Fig. 3(a)], the large injection barrier height (Δ_0) (due to the energy level mismatch described above) prevents electron injection efficiently from the source electrode into the semiconductor layer. When the gate is positively biased [Fig. 3(b)], the capacitor cell is charged up. Negative charge is then built up within the source electrode layer with an exponentially decreasing distribution profile having a maximum at the dielectric/source interface and decreasing toward the source/organic interface. The charge beyond the Debye shielding length[14] is small, but can be amplified by introducing super-high capacitance (such as capacity is above 1 μF/cm^2). Because of the super-high capacitance (25 μF/cm^2 at 25 Hz, 2 V bias, 44% relative humidity) of the capacitor cell, the very thin and rough source layer [roughness is comparable with thickness, as described in Fig. 1(a)], and the possibility of partial oxidization of the source electrode, there is certain amount of negative charge on the top surface of the source electrode of our device. The electric field produced by the charged capacitor cell cannot completely vanish at the source/organic interface due to the rough interface and net charges at the surface, which also induces positive charge in the organic layer, near the source/organic interface. As a result, the electron injection barrier height from the source into the organic layer is lowered by an amount (δ). Hence, the effective energy barrier height (Δ_{eff}) for electron injection from the source electrode is decreased ($\Delta_{eff}=\Delta_0-\delta$), allowing efficient electron injection from the source into the semiconductor layer causing an increase of the source-drain current (I_{sd}) when a drain bias is applied. At a constant drain-source bias (V_d) and temperature (T), the gate potential (V_g) controls the stored charge in the capacitor cell and the δ term. Therefore, V_g controls the effective energy barrier height, $\Delta_{eff}(V_g)=\Delta_0-\delta(V_g)$. Taking the temperature and applied drain bias as constant, it is reasonable to assume that the injection current has an exponential relation with the effective energy barrier, $I(V_g)=I_0*\exp[-\Delta_{eff}(V_g)/(kT)]$, where k is Boltzmann constant, I_0 is a constant.[15,16] It should be mentioned that the electric field produced by the charged capacitor cell at the source/organic interface may also modulate the carrier density and mobility within the organic semiconductor layer, which affects the source-drain *I–V* characteristics. In the VOFETs reported here, we believe that the injection-controlled source-drain current picture (Fig. 3) dominates the device operation mechanism.

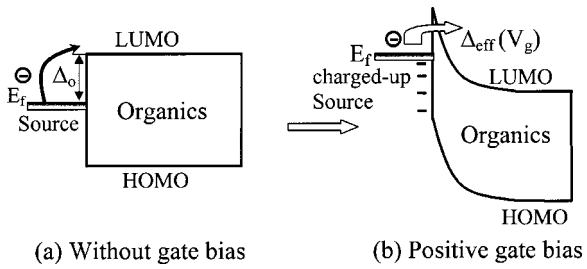

FIG. 3. The schematic band diagram for the VOFET which demonstrates its operating principles: (a) without bias and (b) with positive gate bias.

C_{60} is an *n*-type semiconductor[17,18] which was selected as the organic material. The origin of the injection barrier, shown in Fig. 3, is caused by the mismatch of the metal Fermi level with the lowest unoccupied molecular orbital of C_{60}, so that electrons are transported through an injection barrier from the source electrode to the C_{60} layer.[19] To explain the functional dependence of I_{sd} on V_g in Fig. 2(b), the effective barrier can be mathematically expanded as $\Delta_{eff}(V_g)=\Delta_0-\alpha V_g-\beta V_{g-\ldots}^2$, where Δ_0 and α,β are constants. We found for some region, a liner approximation, $\delta(V_g)=\alpha V_g$, can describe well the $I_{sd}-V_g$ characteristics for some of our devices, where $I_{sd}(V_g)=I_0*\exp[\alpha V_g/(kT)]$. Using this equation we can explain the exponential increase of the I_{sd} with the increase of the gate potential within a certain range. As the gate potential increases, the effective barrier height Δ_{eff} decreases. We found for the data shown in Fig. 3(b) the $\delta(V_g=6\text{ V})$ is about 0.45 eV. One can imagine that above a certain gate voltage Δ_{eff} may reach zero, and the electrons have no injection barrier into the organic layer. In this case, the source-drain current is changed from injection controlled to the bulk controlled, and a saturation shows up in $I_{sd}-V_g$. Moreover, if the stored charge of the capacitor cell is saturated by a high gate voltage, a similar saturation of the source-drain current will also appear.

The current output of our devices is sufficient to drive a organic light-emitting diode (OLED). Figure 4 is a picture which shows a bright OLED driven by a VOFET. The picture was taken in bright room light and the brightness of the organic light-emitting diode (OLED) was about 1000 cd/m^2, sufficient to be an indoor display. The speed of our transistor is mainly determined by the capacitor. Currently, the capacitor speed can go to submillisecond range, which is sufficient to drive active matrix OLED display.[12] In the future, when the size of device shrinks, we anticipate that the VOFET can be even faster, suitable for many other applications.

The bottom capacitor cell of our VOFETs turns out to be a supercapacitor when it is operated in an ambient environ-

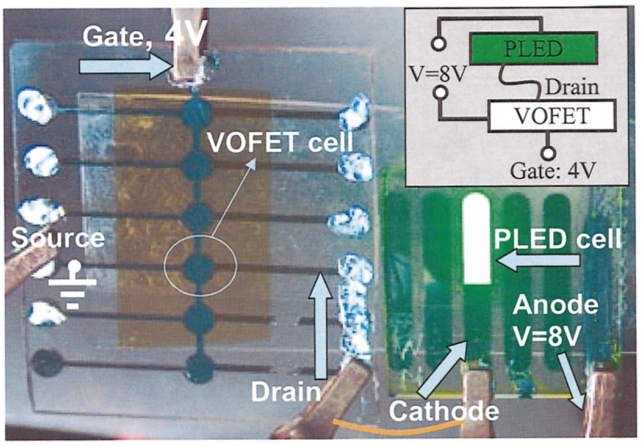

FIG. 4. (Color) The image of an OLED driven by a VOFET. The measurement circuit is shown in the inset. Without gate bias, the 8 V applied to the OLED and the active cell are mainly dropped on the high-resistance active cell, resulting in no light emission from the OLED cell. When a 4 V potential is applied to the gate electrode, the active cell is tuned to low resistance resulting in a 5 V potential drop at the OLED cell, and light emission from the OLED cell with the brightness about 1000 cd/m^2.

ment. A very small amount of LiF in the capacitor cell can be dissolved in a humid environment, leading to the positive and negative ion drift towards the electrodes under bias conditions, where a solid-state double-layer supercapacitor is formed.[20] This argument is supported by the capacitance-frequency measurement [Fig. 1(c)], and the moisture-concentration dependence of the capacitance for the capacitor cell [inset of Fig. 1(c)]. Details about the supercapacitance of our devices are under study. It should be noted that the VOFETs, with LiF as the dielectric layer, only work in a humid ambient that generates a small amount of gate-source current. However, we have also made VOFETs using high-*k* dielectric materials and they work in N_2 environment or vacuum without moisture. Details will be reported in the near future.

The high-capacitance capacitor cell and the very thin and rough source electrode are important for VOFETs. We have prepared half finished VOFETs with relatively thin organic layers on top of the source electrode and without the top electrode. When the gate was biased, we indeed observed charge effects from the organic side by electric force microscopy (EFM) (not shown here). Details about the gate-induced charge effects on the semiconductor layer are under study.

In summary, we have demonstrated a stacked-structure field effect transistor with an active cell on top of a capacitor cell. High-capacitance capacitor cell and very thin and rough source electrode layer are important for device operation. We have obtained organic transistors with low working voltage (less than 5 V), high current output (up to 10 mA or 4 A/cm^2), and high ON/OFF ratio (4×10^6). Our transistors can be incorporated with other organic electronic devices such as organic light-emitting diodes. We have used the transistor as the driver for organic light-emitting diodes and observed controlled emission intensity of the OLED by modulating the gate potential. This device with its enhanced operating characteristics opens directions in basic scientific research for organic transistors and their applications.

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